WHAT IS CLAIMED, IS

1. An apparatus for reading from or writing to optical recording media, comprising a photodetector (10) with at least two detector elements (A, B, C, D), and a phase forming unit (13) for detecting a phase difference (φ) between output signals (A, B, C, D, A+C, B+D) of the photodetector (10), wherein the apparatus further comprises an edge sequence detector (14) for detecting the sequence of edges of the output signals (A, B, C, D, A+C, B+D), and a signal blocking unit (15) for blocking the output signal (φ) of the phase detector (13).

2. The apparatus according to Claim 1, wherein the signal blocking unit (15) blocks a signal which is derived from the output signal (φ) of the phase detector (13) or is used to form this output signal (φ).

3. The apparatus according to Claim 2, comprising diagonal summation signal forming units (11, 12) whose inputs are connected to detector elements (10A, 10B, 10C, 10D) of the photodetector (10) and which output the output signal (A+C, B+D).

4. The apparatus according to Claim 3, comprising edge detectors (21, 21') and phase angle detectors (22, 22'), to which the output signals (A, B, C, D, A+C, B+D) are fed and whose outputs are connected to the phase detector (13) and to the edge sequence detector (14).

5. The apparatus according to Claim 2, comprising edge detectors (21, 21') and phase angle detectors (22, 22'), to which the output signals (A, B, C, D, A+C, B+D) are fed and whose outputs are connected to the phase detector (13) and to the edge sequence detector (14).

6. The apparatus according to Claim 1, comprising diagonal summation signal forming units (11, 12) whose inputs are connected to detector elements (10A, 10B, 10C, 10D) of the photodetector (10) and which output the output signal (A+C, B+D).

7. The apparatus according to Claim 1, comprising edge detectors (21, 21') and phase angle detectors (22, 22'), to which the output signals (A, B, C, D, A+C, B+D) are fed and whose outputs are connected to the phase detector (13) and to the edge sequence detector (14).

8. The apparatus according to one of Claim 1, wherein the phase forming unit (13) and the edge sequence detector (14) are integrated.

9. The apparatus according to claim 1, comprising a fault indicator (25), which is connected to an output of the edge sequence detector (14).

10. A method for determining a correct track error signal (TE) in accordance with a phase detection method, comprising the steps of checking of the sequence of zero crossings (a, b) of signals (A, B, C, D, A+C, B+D), whose phase is detected, with regard to impermissible sequences, and preventing the outputting of a phase value (φ) when an impermissible sequence is present.

11. The method of Claim 10, wherein a sequence of more than two successive zero crossings of one signal (A, B, C, D, A+C, B+D) without the occurrence of a zero crossing in the other signal (A, B, C, D, B+D, A+C) is an impermissible sequence.

12. The method of Claim 10, wherein a sequence of more than one pair of zero crossings within a

predetermined time period, a pair of zero crossings consisting of a zero crossing of one signal (A, B, C, D, A+C, B+D) and a succeeding zero crossing of the other signal (A, B, C, D, B+D, A+C), is an impermissible sequence.

13. The method of Claim 10, wherein an error indication signal (FI) is generated as a function of the accumulation of impermissible sequences.

14. The method of Claims 10, wherein the signals (A, B, C, D, A+C, B+D) are evaluated in a predetermined clock cycle (T), a zero crossing (a, b) being present if one of two successive values (a_n, a_{n-1}, b_n, b_{n-1}) of the signal (A, B, C, D, A+C, B+D) lies above, and the other of the said values lies below, a reference value (SL1, SL2), and the temporal position of the zero crossing (a, b) is interpolated using these two values (a_n, a_{n-1}, b_n, b_{n-1}).

15. The method of Claim 14, wherein the phase (φ) between a zero crossing (a, b) of one signal (A, B, C, D, A+C, B+D) and a zero crossing (b, a) of the other signal (A, B, C, D, B+D, A+C) is determined from the respective interpolated temporal position (t_1, t_2) and the number of clock cycles (T_A) lying between the zero crossings (a, b).

16. The method of Claim 10, comprising the step of extrapolating the track error signal (TE) in the event of an impermissible sequence.

17. The method of Claim 10, wherein the phase detection method is the differential phase detection method, the signals to be compared being the diagonal summation signals (A+C, B+D).